MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL
(Formerly WEST BENGAL UNIVERSITY OF TECHNOLOGY)
Main Campus: NH 12, Haringhata, P.O. - Simhat, Police Station – Haringhata, Nadia-741249
City Campus: BF-142, Sector -I, Salt Lake, Kolkata -700 064

Advt. No. MAKAUT/REG/Project Assoc-I/10 **Dated, 08/04/2025**

Applications are invited from Indian citizens for **Project Associate-I** for the MeitY sponsored project in the Department of Microelectronics and VLSI Technology, MAKAUT, WB, Haringhata, Nadia, West Bengal - 741249, India with the details mentioned below:

Project Details:

Title of the Project	"Analog Digital Mix Signal Processor- A novel architecture for signal processing"
Sponsored Agency	Ministry of Electronics & Information Technology (MeitY), Government of India, under C2S.
Position Title	**Project Associate-I**
No. of Position	Two (02)
Tenure of the project	Up to February 2027
Duration	Initially for one year or till the end of the financial year (annually extendable till the end of the project subject to satisfactory performance)
Age limit	Upper Age limit 35 years

Other Details:

1	Name of Project Investigator (PI)	CI: Dr. Mihir Kumar Mahata, Associate Professor (C), Microelectronics and VLSI Technology, MAKAUT, WB.
2	Fellowship & HRA	(i) Fellowship: Rs.31,000/- + HRA (As per University norms) to Scholars whom are selected through (a) National Eligibility Tests – CSIR-UGC NET including lectureship (Assistant Professorship) or GATE or (b) A selection process through National level examinations conducted by Central Government and their Agencies and Institutions. (ii) 25,000/- + HRA (As per University norms) for others who do not fall under (i) above.
3	Essential Qualifications	(i) ME/M Tech in Electronics & Communication Engineering/Microelectronics & VLSI Technology/ Embedded System/ VLSI Design/ EE/AEIE/CSE/EEE/IT/M Sc in Electronics with 60% marks or CGPA of 6.75 and above. Should have CSIR-UGC NET/GATE (ii) ME/M Tech in Electronics & Communication Engineering/ Microelectronics & VLSI Technology/Embedded System/VLSI Design/EE/AEIE/CSE/EEE/IT/M Sc in Electronics with 60% marks or CGPA of 6.75 and above.
4	Desirable	Knowledge of EDA tools, Chip Design, LINUX, etc. Knowledge of VLSI design
5	Important Instructions	• The assignment is purely temporary and it is coterminous with the project. • All original testimonials would be required to be produced for verification purposes at the time of interview/joining. • No TA/DA will be paid for appearing in the interview and joining the position. • All the terms & conditions for this recruitment will be as per the guidelines of MeitY.

		• Only shortlisted candidates will be intimated via e-mail. Candidates are advised to check their emails regularly.
6	How to Apply	• Send your CV along with all the relevant documents about the details of qualifications, age, email, mobile number, experience, etc., on or before 16/05/2025 in the below link and send your filled application form in pdf format (scan) in the application format enclosed to e-mail ID: mihirkumar.mahata@makautwb.ac.in • And fill the Google form via the link mentioned below: https://forms.gle/irJBKZvUw9nEjUM59 Shortlisted candidates will be called for an interview at a later date which will be intimated by e-mail.

Registrar
MAKAUT, WB

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Application for the post of.....

1. Name: .....
2. Father's Name: .....
3. Date of Birth: .....
4. Contact information:
   (i)Telephone with STD Code:.....(ii) Mobile No: .....

   (iii) Address for Communication .....

   .....

   (iv) e-mail ID: .....
5. Educational Qualifications:

Class	Discipline	Board/ University	Name of the school/ Institute	Marks Scored (% of CGPA)	Year of Passing
$_{10}$th					
$_{12}$th					
Graduation					
Post-Graduation					
Ph.D.					
Others					

6. GATE/NET/ ICMR/ DBT-SRF score earned/qualified:

Score	Year appeared	Score	All India rank
GATE/NET			

7. Experience (Details): (Attach a separate sheet if required)

Organization	Designation	Date/Month of entry	Date/Month of leaving	Responsibilities

8. Total Experience (in years).....
9. Publications, if any: (Attach a separate sheet if required)

   National (Nos) .....International(Nos) .....

10. Patents, if any (Attach a separate sheet if required) :

11. Workshop/Training programs attended.....
(Attach Separate Sheet with tabular entry if required)

12. Other qualifications/Certified course/relevant information/achievements if any

S. No.	

Declaration:

I …… hereby declare that all statements made in this application are true, complete and correct to the best of my knowledge and belief. In the event of the information being found false or incorrect or any ineligibility being detected before or after the selection, my candidature is liable to be cancelled.

Date: **Signature of applicant with name**

Note:

- Please attach an attested photocopy of supporting documents for columns 5 to 11 along with the application form.
- Original Certificates for verification with one photocopy to be brought at the time of the interview only.
- Send your filled application form in pdf format (scan) to both of the email IDs: mihirkumar.mahata@makautwb.ac.in sowvik.dey@makautwb.ac.in