



**Indian Institute of Technology (Indian School of Mines), Dhanbad**  
The Office of Dean, Research & Development

Sanction No and Date: TTDF/6G/162 Dated:26/06/2025	<b>IIT (ISM) Dhanbad Project No.</b> SRDP 1176G	Date 31/12/2025
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**Junior Research Fellow (JRF) position under the TTDF scheme of DBN (DoT) and assigned to TCOE India as the implementing agency by the competent authority.**

The details are given below:

<b>Position</b>	Junior Research Fellow (JRF)
<b>Number of Position (s)</b>	1
<b>Title of The Project</b>	Silicon Photonic Chip-based N × N Photonic Switches for 6G and Beyond
<b>Principal Investigator</b>	Prof. Devendra Chack, Associate Professor, Department of Electronics Engineering, IIT(ISM) Dhanbad, Jharkhand 826004. Email: <a href="mailto:devendra@iitism.ac.in">devendra@iitism.ac.in</a> .
<b>Tenure of Project</b>	The initial appointment will be for 1 year. The contract will be renewable, subject to satisfactory performance and project requirements. (Maximum three years or till the end of the project, whichever is earlier) Opportunity Highlights: JRF will have the chance to apply for a PhD position in the Department of Electronics Engineering, IIT (ISM) Dhanbad, following institute guidelines.
<b>Job Description (in maximum of 100 words)</b>	The project aims to design Silicon Photonic Chip-based N × N Photonic Switches for 6G and Beyond. Specifically, the project has the following goals: 1) To design an integrated Silicon Photonic N × N optical switch 2) To validate performance through simulation (FDTD/INTERCONNECT) 3) To prepare fabrication-ready layouts (PDK/KLayout) following foundry design rules. 4) Device and System-level Characterization
<b>Essential Qualification</b>	First Class or First Division with minimum 60% marks or equivalent CGPA in M. Tech. / M.E. / MS in Electronics / Electronics & Communication / Electronics & Telecommunication or related field [OR] B. Tech / B.E. or equivalent degree in Electronics / Electronics & Communication / Electronics & Tele-communication [OR] M.Sc in Electronics, [OR] M.Sc in Physics (Specialization in Electronics/Photonics). The candidate must have qualified GATE/NET.
<b>Desirable Qualification</b>	The candidate should have basic knowledge of Photonics Integrated Circuits, Silicon Photonics and Communication systems, Microelectronics, Optoelectronics, Nanotechnology, Optical Communication, VLSI or Physics from a recognized institute. Furthermore, the candidate should be good at ANSYS Lumerical and MATLAB.
<b>Age and Relaxation (if any)</b>	35 years at the time of appointment. A relaxation in the upper age limit will be given to SC/ST/OBC (Non-creamy layer)/PH candidates as per GOI rule.
<b>Fellowship</b>	<b>Rs. 37,000/- for the 1<sup>st</sup> and 2<sup>nd</sup> Year, and Rs. 42,000/- for 3<sup>rd</sup> Year</b>
<b>Last Date &amp; Time</b>	<b>20th January 2026 (Tuesday), 04:00 PM.</b> Interested and eligible candidates should email a single PDF containing the Form/Biodata/CV, Self-attested copies of all the marksheets and certificates starting from 10th standard, GATE/NET score card, age proof, caste certificate (if applicable), work experience (if any) to the principal investigator at <a href="mailto:devendra@iitism.ac.in">devendra@iitism.ac.in</a> within the above deadline.
Shortlisted candidates will be informed on the date of interview. Mere possession of minimum qualification does not guarantee an invitation to the interview. Candidates will be shortlisted based on their merit and as per the requirement of the project. All candidates should make their own arrangements for their stay at Dhanbad, if required. No TA/DA will be paid to attend the interview.	

**(Signature of PI)**

**Application Form for Junior Research Fellow (JRF) position under the TTDF scheme of DBN (DoT) “Silicon Photonic Chip-based N × N Photonic Switches for 6G and Beyond”, under Prof. Devendra Chack, Associate Professor, Department of Electronics Engineering, IIT(ISM) Dhanbad.**

Full Name (In block letters):

Father's Name:

Sex:

Marital Status:

Date of Birth & Age:

Correspondence address:

Permanent Address:

Contact number:

Email ID:

Affix a  
Passport size  
photo

\*Details of academic & technical qualifications (High School and above, starting from recent):

S.No.	Qualification	Name of Board/University	Year of Passing	Percentage of Marks
1.				
2.				
3.				
4.				
5.				

\*Details of Work/Research Experience (After obtaining eligible qualification):

S. No.	Post	Name of the Institution	From (DD/MM/YY)	To (DD/MM/YY)	Total Experience	Duties & Responsibility
1.						
2.						

*\*(Attach the self-attested copies of educational qualifications, work/research experience and publications)*

Details of Publications:

Author(s) Name	Title	Journal /Conference Name	Vol.	Year of Publication

Present employment (if any): \_\_\_\_\_

**Declaration:**

I hereby declare that the above-mentioned details are true, complete, and correct to the best of my knowledge and belief. In case anything furnished by me ultimately turns out to be false, it will lead to the cancellation of my candidature.

Date:

Place:

Name:

(Signature)

**Enclosure attached:**

- 1.
- 2.
- 3.
- 4.
- 5.