INDIAN INSTITUTE OF TECHNOLOGY PATNA
BIHTA PATNA-801106
RESEARCH & DEVELOPMENT UNIT

ADVERTISEMENT NO: R&D/908/MEM/607 **DATED: 09.07.2026**

Project No. **R&D/SP/EE/MEM/2023-24/908**

Applications are invited in the prescribed format only for the following assignment in a purely time bound research project undertaken in this institute.

1. (a) Name of the temporary assignment: Junior Research Fellow (JRF)

(b) Number of Post : 01 (One)

(c) Duration of the Post : 02 (Two Years) as JRF, thereafter Senior Research Fellow (SRF) till completion of the project

(d) Duration of the Project : ThreeYear (May extend to another one year)

2. Name of the temporary research project : *ML Enabled RISC-V based i-LoRa SOC for Forest Event Monitoring*

3. Broad Research Domain : VLSI Architectures for edge computing system / Communication Systems/ Machine Learning.

4. Name of the sponsoring Agency : Ministry of Electronics and Information Technology (MeitY), Delhi under C2S Programme

5. Consolidated Fellowship/Salary : Rs. 37000 (for JRF) and Rs. 42000 (for SRF)

6. **Qualification** : **M. Tech. / B. Tech./M.Sc. (Electrical /Electronics / Communication/ Instrumentation / Computer Science & Engineering)**

The candidate desirably should have **M. Tech**.(VLSI/Embedded System/Microelectronics/ Electronics System/Communication System/Instrumentation and Computer Science Engineering) degree with a minimum CPI of 6.5 or 60% of marks with qualified GATE Score (within last five years) **OR B.Tech/B.Sc(Engg.)/M.Sc.**(Electrical/Electronics/Communication/Instrumentation/ Computer Science& Engineering) degree with a minimum CPI of 7.5 or 70% of marks with **qualified GATE Score within last five years**. GATE score shall be exempted for candidates having B. Tech degree with minimum CPI 7.5 from IITs. Exceptional candidates having M. Tech degree and minimum two (02) years of relevant experience, may be offered SRF Position directly based on the performance in interview. The upper age limit for applying for the JRF position shall be **32 and 28 years** for candidates having M. Tech and B. Tech/B.Sc.(Engg.)/M.Sc. degree respectively on the date of advertisement.

Relaxations for SC/ST/OBC/women/PD will be given as per the GOI rules. Working/research experience in the field of **VLSI and Embedded System/ Computer Architecture/ Communication System/Machine Learning and exposure to EDA tools** shall be given preference. **Selected candidate shall be admitted to PhD program in Electrical Engineering Department, IIT Patna in Spring-2026 based on the rules and regulation of the institute.**

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Suitable candidates having exposure/experience in these domain and not having GATE score shall be considered only for JRF Position in aforesaid project.

Interested and eligible candidates may send the scan copy of **application form (in appended format) and GATE Score Card** along with **resume** highlighting the relevant exposure in the domain of the project to the mail id: kcr@iitp.ac.in. on or before ***7th August 2026***. Shortlisted candidates shall be intimated on ***8th August 2026*** and called for the **Written test** and **PERSONAL INTERVIEW** to be scheduled on **21st August *2026***, Timing **10 AM** at Dept. of Electrical Engineering, IIT Patna, Bihta, Patna – 801106 with updated resume along with the original copies of all supporting documents (certificates, mark-sheets, and GATE Score card).

Second Class Train fare in shortest route shall be admissible for appearing the personal interview in physical mode at IIT Patna. Guest room in student hostel may be arranged on prior intimation through mail for maximum two days only.

Tentative Important Dates:

Last date for receiving the application form through mail : 7th August 2026
Date of intimation of shortlisted candidates through mail : 8th August 2026
Date of Personal Interview : 21st August 2026

Please Note that, candidates those are willing to pursue PhD in the domain of VLSI & Embedded System in Electrical Engineering Department, are only encouraged to apply this JRF/SRF position subject to the fulfil of the PhD admission protocol of the department and institute.

For any query. please contact Principal Investigator of the Project: **Dr. Kailash Chandra Ray, Dept. of Electrical Engineering, IIT Patna, Email: kcr@iitp.ac.in**

Assistant Registrar (R&D)

Copy to:
1. Associate Dean, R&D, IIT Patna
2. PIC (Outreach) to put it in institute social media channel
3. Advertisement file
4. Project file

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ADVT NO: R&D/908/MEM/607 **DATED: 09.07.2026**

FORMAT OF APPLICATION FOR …JRF/SRF…….

Name & Address **Including email id and Phone no. (for Correspondence)**	**Category** (GEN/OBC/SC/ST/PD)	**DOB** dd/ mm/yy	**Professional Exam. (GATE/CSIR-NET, etc) , Specialization(EE/EC/IN/CS), and GATE Score and rank along with the year of GATE Score**
NAME IN CAPITAL Address: Phone: Email:			

Educational Qualification

Institute/ Board	**Exam Passed**	**Year of Passing**	**% of Marks/CPI**
	10th Class		
	12th Class		
	Bachelors (B.Tech/B.E.)/M.Sc. or equivalent		
	Masters (M.Tech/M.E) or equivalent		

Qualifying degree	**Degree/ major/Specialization**
(B.Tech/B.E./M.Sc.)	
(M.Tech/M.E)	
Others	

Signature of applicant

Date:
Place: